Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.254”**

**SOURCE**

**GATE**

**.248”**

**Top Material: Al**

**Backside Material: Cr Ni Ag**

**Bond Pad Size: S= .051 X .037” G= .027 X .019”**

**Backside Potential: Drain**

**Mask Ref: GEN 3**

**APPROVED BY: DK DIE SIZE .248” X .254” DATE: 7/14/17**

**MFG: INT’L RECTIFIER THICKNESS .010” P/N: IRFC450**

**DG 10.1.2**

#### Rev B, 7/1